## In the Specification

At page 1, please amend the paragraph before the "Technical Field" section as follows:

## RELATED PATENT DATA

This patent application is a Divisional Application of and claims priority to U.S. Patent Application Serial No. 10/459,064, filed July June 10, 2003, entitled "Computer Systems, Processes For Forming A SRAM Cell, Processes For Turning A SRAM Cell Off, Processes For Writing A SRAM Cell and Processes for Reading Data From a SRAM Cell," naming Leonard Forbes as inventor which is a Divisional Application of U.S. Patent Application Serial No. 10/202,551, filed July 23, 2002, entitled "A Four Terminal Memory Cell, A Two-Transistor SRAM Cell, A SRAM Array, A Computer System, A Process For Forming A SRAM Cell, A Process For Turning A SRAM Cell Off, A Process For Writing A SRAM Cell and A Process for Reading Data From a SRAM Cell," naming Leonard Forbes as inventor, which is a Divisional Application of U.S. Patent Application Serial No. 09/941,369, filed August 28, 2001, entitled "A Four Terminal Memory Cell, A Two-Transistor SRAM Cell, A SRAM Array, A Computer System, A Process For Forming a SRAM Cell, A Process For Turning a SRAM Cell OFF, A Process for Writing a SRAM Cell and A Process For Reading Data From a SRAM Cell," naming Leonard Forbes as inventor, the disclosure disclosures of which [[is]] are hereby incorporated herein by reference.